CJC5357B

96KHz 24-Bit Sampling ΔΣADC

Data Sheet

Contents

1. General Discription

The CJC5357B is a sampling rate 4KHz ~ 96KHz stereo ADC, it is suitable for multi-media audio systems. CJC5357B with enhanced dual-bit -Σ technology, owns high precision and low power consumption properties. Because it is a single-ended input devices, there is no need for additional devices. The audio interface supports two formats (MSB justified, I2S), and can be used in a variety of systems, such as karaoke OK, surround sound and so on.

2. Features

- □ Stereo Δ-Σ ADC
- □ On-chip digital anti-alias filter
- □ Single-ended input
- □ Digital high-pass filter to eliminate DC offset
- □ S/(N+D): 84dB@3.3V for 48kHz
- □ DR: 99dB@3.3V for 48kHz
  98dB@3.3V for 96kHz
- □ S/N: 99dB@3.3V for 48kHz
  98dB@3.3V for 96kHz
- □ Sampling Rate: 4kHz ～ 96kHz
- □ Master Clock:
  256fs/384fs/512fs/768fs (4kHz~48kHz)
  256fs/384fs (48kHz~96kHz)
- □ CMOS Input Level
- □ Master/Slave mode
- □ Audio Interface: 24bit MSB justifed/I2S is optional .
- □ Power Supply: 2.7 to3.6V
- □ Ta= —40~85℃（industrial）, Ta=—20~85℃（commercial）
- □ Package:16pin TSSOP

3. Diagram

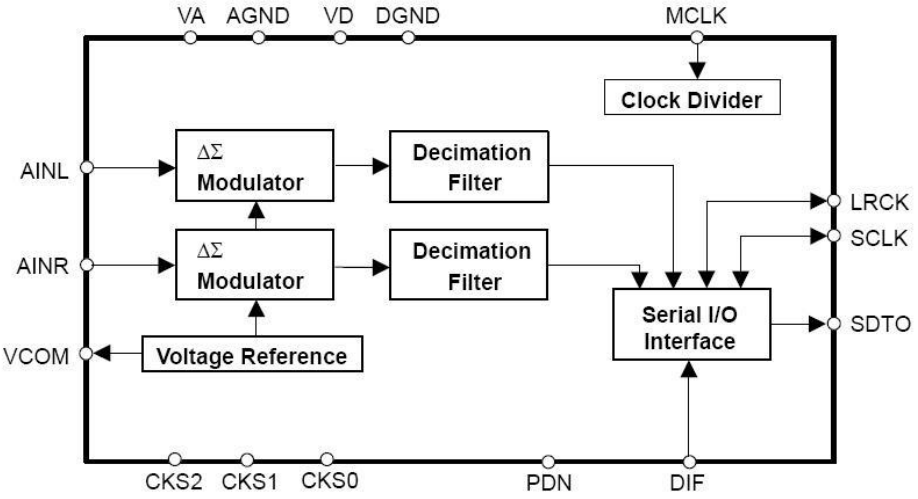

Figure 1. CJC5357B diagram

4. Pin Layout

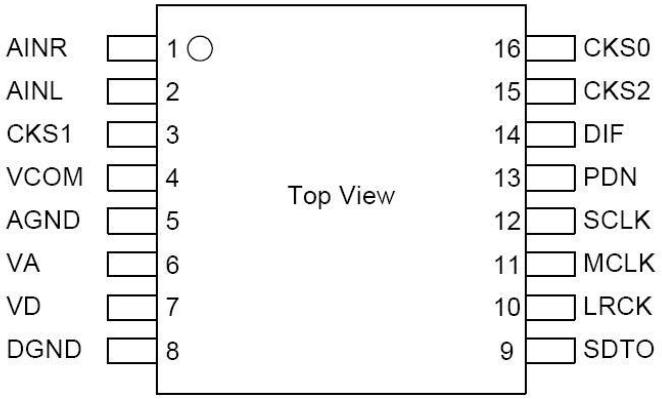

Figure 2. CJC5357B Top View

5. Pin/Function

NO.	Pin Name	I/O	Function
1	AINR	I	Rch Analog Input Pins
2	AINL	I	Lch Analog Input Pins
3	CKS1	I	Mode Select 1 Pin
4	VCOM	O	Common Voltage Output Pin, VA/2 Bias Voltage of ADC Input
5	AGND	-	Analog Ground Pin
6	VA	-	Analog Power Supply Pin，.7~3.6V
7	VD	-	Digital Power Supply Pin, 2.7~3.6V
8	DGND	-	Digital Ground Pin
9	SDTO	O	Audio Serial Data Output Pin “L” Output at Power-down mode
10	LRCK	I/O	Output Channel Clock Pin “L” Output in Master Mode at Power-down mode
11	MCLK	I	Master Clock Input Pin
12	SCLK	I/O	Audio Serial Data Clock Pin “L” Output in Master Mode at Power-down mode
13	PDN	I	Power Down Mode Pin “H”:Power up，“L”：Power down
14	DIF	I	Audio Interface Format Pin “H”：24bit I^2S Compatible , “L”:24 bit MSB justified
15	CKS2	I	Mode Select 2 Pin
16	CKS0	I	Mode Select 0 Pin

Note: All digital input pins should not be left floating .

5.1. Handling of Unused Pin

The unused input pins should be processed appropriately as below:

Classification	Pin Name	Setting
Analog	AINL	This pin should be open
	AINR	This pin should be open

6. Electrical Characteristics

6.1. Absolute Maximum Ratings

Parameter		Symbol	Min	Max	Units
Power Supplies	Analog	VA	−0.3	6.0	V
	Digital	VD	−0.3	6.0	V
	|AGND−DGND| (Note 2)	ΔGND	-	0.3	V
Input Current,（Any Pin Except Supplies）		IIN	-	±10	mA
Analog Input Voltage（AINL, AINR,CKS1 pins）		VINA	−0.3	VA+0.3	V
Digital Input Voltage（All digital input pins except KS1 pin）		VIND	−0.3	VD+0.3	V
Ambient Temperature		Ta	−20	85	℃
		Ta	−40	85	℃
Storage Temperature		Tstg	−65	150	℃

Note 1：All voltage with respect to ground.

Note 2：AGND and DGND must be connected to the same analog ground plane. Warning：Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

6.2. Recommended operation conditions

（AGND,DGND=0V;Note 1）

Parameter		Sybol	min	typ	max	Units
Power Supplies	Analog	VA	2.7	3.3	3.6	V
（Note 3）	Digital	VD	2.7	3.3	3.6	V

Note 3：The power up sequence between VA and VD is not critical .

Warning ： LuHua Semiconductors a ssume s no responsibility for the usage beyond the conditions in this datasheet .

6.3. Analog Characteristics

（ Ta=25℃; VA=VD=3.3V; AGND=DGND=0V; fs=48kHz,96kHz; Signal Frequency=1kHz; 24bitData; Measurement Frequency=20Hz~20k Hz at fs=48kHz,40Hz~40k Hz at fs=96kHz;unless otherwise specified ）

Parameter			Min	Typ	Max	Units
ADC Analog Input Characteristics						
Resolution					24	Bits
Input Voltage （Note 4）		VA=3.3V	-	1.98	-	
S/(N+D) (－1DBFS)	VA=3.3V	fs=48kHz	-	84		dB
		fs=96kHz	-	76		dB
DR （－60DBFS)	VA=3.3V	fs=48kHz,A-weighted	-	99		dB
		fs=96kHz	-	98		dB
S/N	VA=3.3V	fs=48kHz,A-weighted	-	99		dB
		fs=96kHz	-	98		dB
Input Resistance		fs=48kHz	13	20		kΩ
		fs=96kHz	9	14		
Interchannel Isolation			94	100		dB
Interchannel Gain Mismatch				0.1	0.5	dB
Gain Drift				100	-	ppm/ ℃
Power Supply Rejection （Note 5）				54		dB
Power Supplies						
Power Supply Current						
Normal Operation						
VA				7	8.5	mA
VD (fs=48kHz)		(Note 6)		1.5	3	mA
VD (fs=96kHz)		(Note 7)		2	4	mA
Power down mode (PDN pin="L")		(Note 8)		1	100	μA
VA+VD						

Note 4：This value is the full scale of the input voltage .Input voltage is proportional to VA voltage . Vin=0.6×VA(Vpp)

Note 5：PSR is applied to VA and VD with 1 kHz，50mVpp.

Note 6：VD=1.5mA@3.3V

Note 7：VD=2mA@3. 3V

Note 8： All digital input pins are held VD or DGND.

6.4. Filter Characteristics

(1) (Ta=Tmin~Tmax;VA,VD=2.7~3.6V，fs=48k Hz)

Parameter		Sybol	Min	Typ	Max	Units
ADC Digital Filter (Decimation LPF)						
Passband	±0.02dB −3.5 dB	PB	0 -	23.0	20	kHz kHz
Stopband		SB	28			kHz
Passband Ripple		PR			±0.02	dB
Stopband Attenuation		SA	66			dB
Group Delay Distortion		△GD		0		μ S
Group Delay （Note 9）		GD		13		1/fs
ADC Digital Filter (HPF)						
Frequency Response	−2.7 dB −0.1dB	FR		1.0 6		Hz Hz

(2)(Ta=Tmin~Tmax;VA,VD=2.7~3.6V，fs=96kHz)

Parameter		Sybol	Min	Typ	Max	Units
ADC Digital Filter (Decimation LPF)						
Passband	±0.02dB −3.5 dB	PB	0 -	46.0	20	kHz kHz
Stopband		SB	56			kHz
Passband Ripple		PR			±0.02	dB
Stopband Attenuation		SA	66			dB
Group Delay Distortion		△GD		0		μ S
Group Delay （Note 9）		GD		13		1/fs
ADC Digital Filter (HPF)						
Frequency Response	−2.7 dB −0.1dB	FR		2.0 12		Hz Hz

Note 9： The calculated delay time is induced by digital filtering .This time is from the input of an analog signal to the setting of 24bit data both channels to the ADC input register for ADC.

6.5. DC Characteristics

(1) CMOS Level Mode

(Ta=Tmin~Tmax;VA,VD=2.7~5.5V，CMOS Level)

Parameter	Sybol	Min	Typ	Max	Units
High-level Input Voltage	VIH	70%VD	-	-	V
Low-level Input Voltage	VIL	-	-	30%VD	V
High-level output Voltage (Iout=－1mA)	VOH	VD－0.5	-	-	V
Low-level output Voltage (Iout=1mA)	VOL	-	-	0.5	V
Input Leakage Current	Iin	-	-	±10	μA

(2) Switching Characteristics

(Ta=Tmin~ Tmax;VA,VD=2.7~3.6V ； C_L =20pF)

Parameter			Sybol	Min	Typ	Max	Units
Master Clock Time							
Frequency			fCLK	1.024		36.684	MHz
Pulse Width Low			tCLKL	0.4/fCLK			ns
Pulse Width High			tCLKH	0.4/fCLK			ns
LRCK Frequency			fs	4		96	kHZ
	Duty Cycle	Slave Mode		45		55	%
		Master Mode			50		%
Audio Interface Timing							
	Slave Mode						
	SCLK Period		tSCK	160			ns
	SCLK Pulse Width Low		tSCKL	65			ns
	Pulse Width High		tSCKH	65			ns
	LRCK Edge to SCLK“↑” （Note 11）		tLRSH	30			ns
	SCLK“↑”to LRCK Edge （Note 11）		tSHLR	30			ns
	LRCK to SDTO (MSB) (ExceptI2S mode)		tLRS			35	ns
	SCLK“↓”to SDTO		tSSD			35	ns
	Master Mode						
	SCLK Frequency		fSCK		64fs		Hz
	SCLK		dSCK		50		%
	SCLK“↓”to LRCK		tMSLR	－20		20	ns
	SCLK“↓”to SDTO		tSSD	－20		35	ns

Reset 时序					
PDN Pu lse Width （Note 12）	tPD	150			ns
PDN“↑”to SDTOvalid at Slave Mode（Note 13）	tPDV		4233		1/fs
PDN“↑”to SDTOvalid at Maste Mode（Note 13）	tPDV		4051		1/fs

Note 11：SCLK rising edge must not occur at the same time as LRCK edge.

Note 12：The CJC5357B can be reset by bringing the PDN pin=”L”.

Note 13：This cycle is the number of LRCK rising edge from the PDN pin=”H”.

7. Timing Diagram

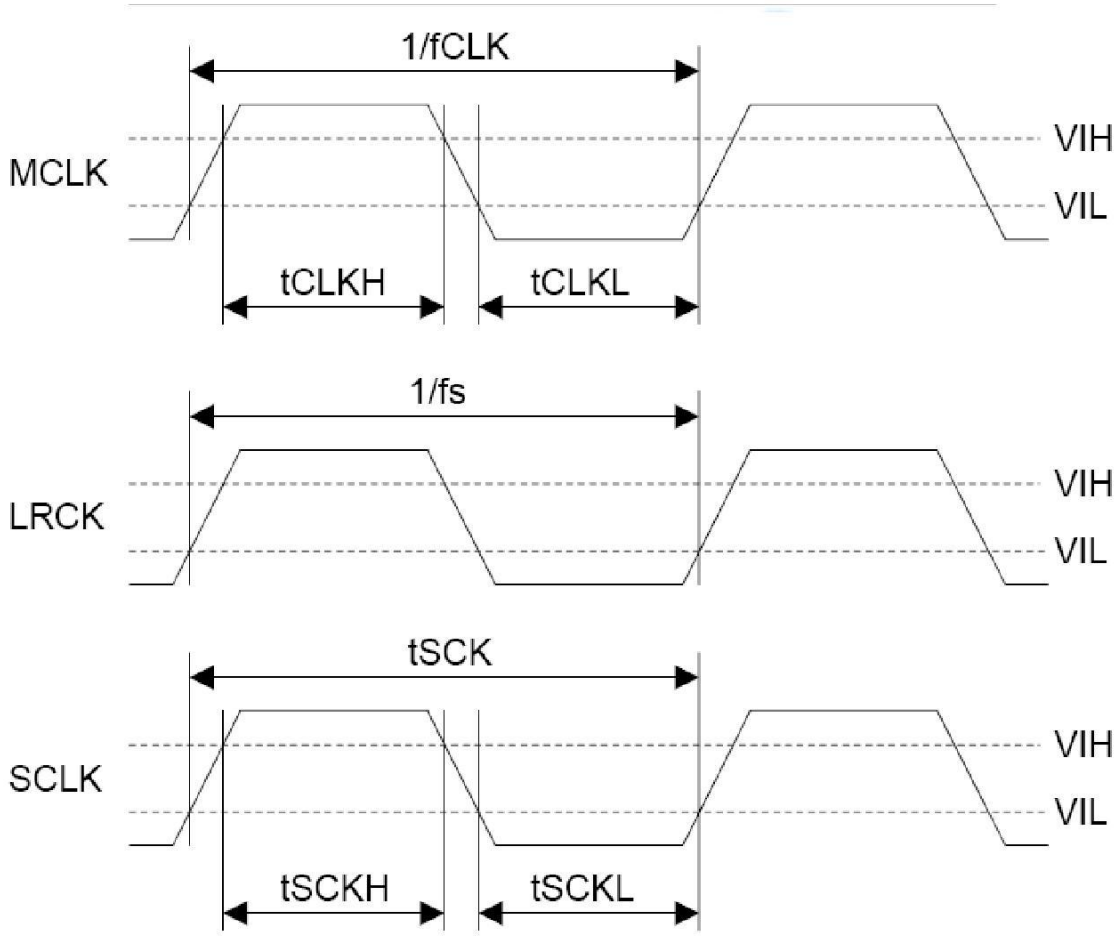

Figure 3. MCLK，LRCK，SCLK Clock Timing

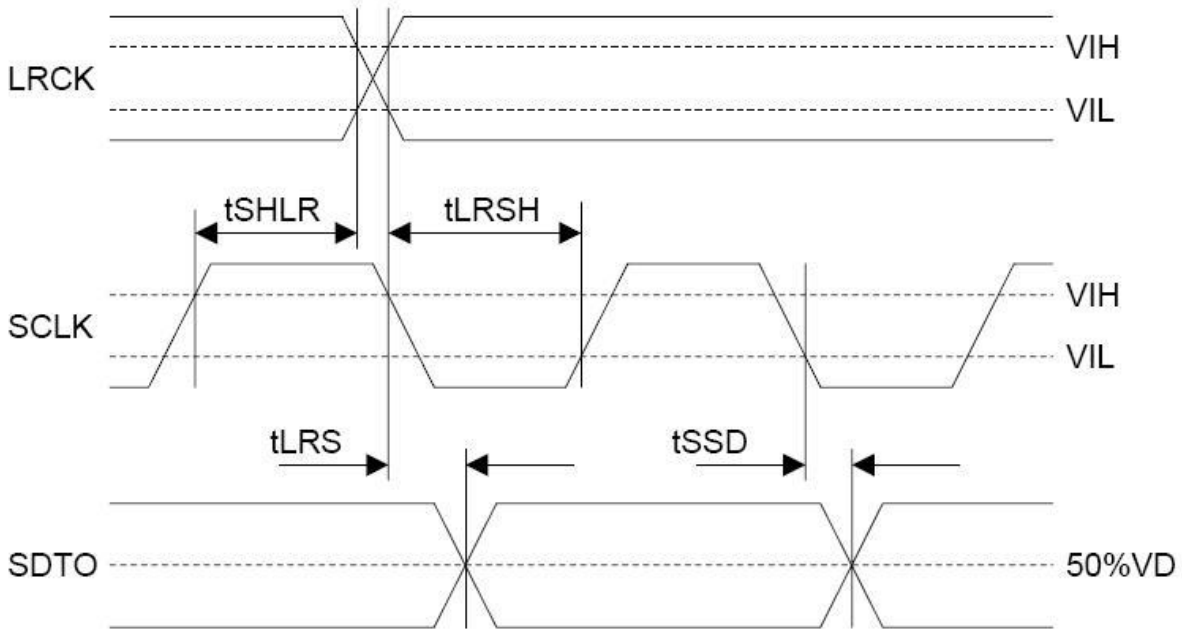

Figure 4 Audio Interface Timing（Slave Mode）

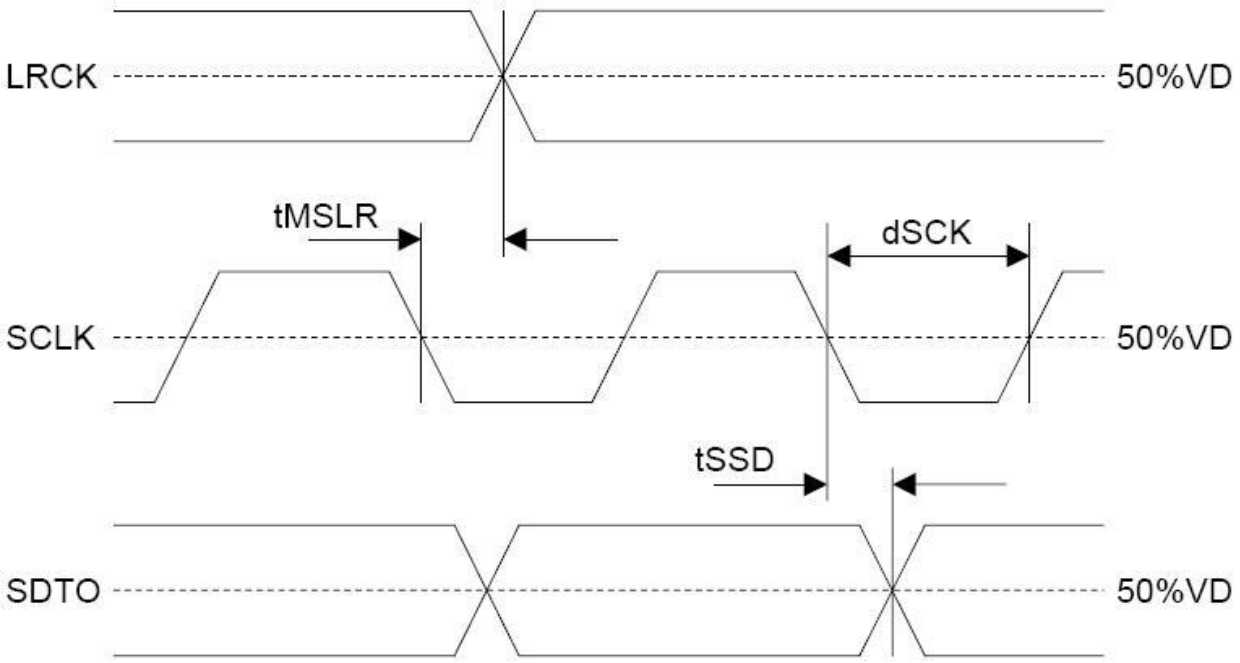

Figure 5. Audio Interface Timing（Master Mode）

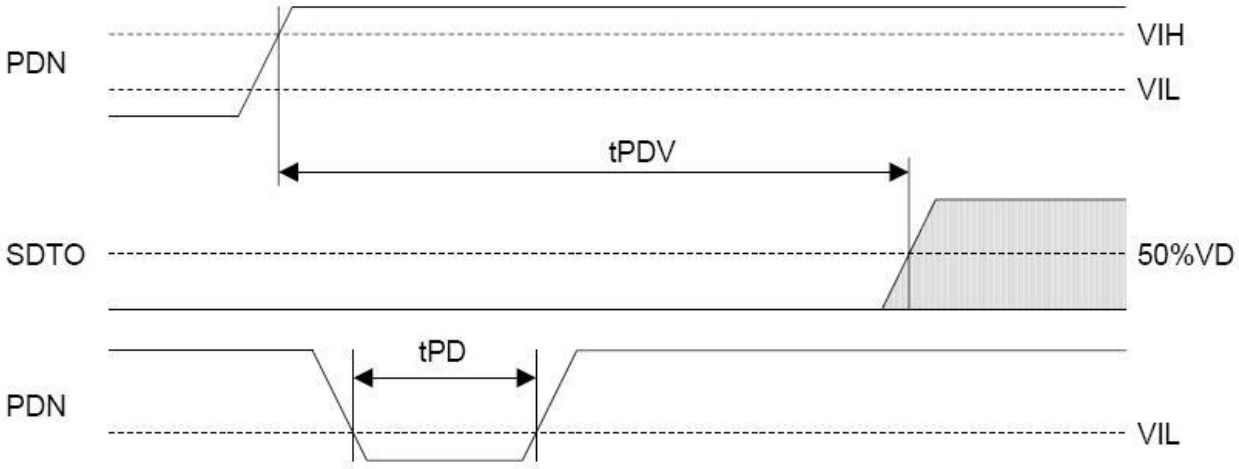

Figure 6. Reset Timing

8. Operation Overview

8.1. System Clock

In slave mode,MCLK(256fs/384fs/512fs),SCLK and LRCK clocks are required. The LRCK clock input must be synchronized with MCLK,however the phase is not critical.Table 1 shows the relationship of typical samplig frequency and the system clock frequency. MCLK frequency, SCLK frequency ,HPF(ON or OFF)and master/slave mode are selected by CKS2-0 pins as shown in Table 2.

All extemal clocks (MCLK, SCLK,and LRCK)must be present unless the PDN pin="L". If these clocks are not provided,the CJC5357B may draw excess current due to its use of internal dynamically refreshed logic. If the extemal clocks are not present,place the CJC5357B in power-down mode(PDN pin="L"). In master mode ,the master clock(MCLK)must be provided unless the PDN pin="L".

fs	MCLK			
	256fs	384fs	512fs	768fs
32kHz	8.192MHz	12.288MHz	16.384MHz	24.576MHz
44.1kHz	11.2896MHz	16.9344MHz	22.5792MHz	33.8688MHz
48kHz	12.288MHz	18.432MHz	24.576MHz	36.864MHz
96kHz	24.576MHz	36.864MHz	N/A	N/A

Table 1：System Clock Example

CKS2	CKS1	CKS0	HPF	Master/Slave	MCLK	SCLK
L	L	L	ON	Slave	256/384fs (~ 96kHz) 512/768fs (~ 48kHz)	≥ 48fs or 32fs
L	L	H	OFF	Slave	256/384fs (~ 96kHz) 512/768fs (~ 48kHz)	≥ 48fs or 32fs
L	H	L	ON	Master	256fs (~ 96kHz)	64fs
L	H	H	ON	Master	512fs (~ 48kHz)	64fs
H	L	L	ON	Slave	256/384fs (~ 96kHz) 512/768fs (~ 48kHz)	≥ 48fs or 32fs
H	L	H	Reserved			
H	H	L	ON	Master	384fs (~ 96kHz)	64fs
H	H	H	ON	Master	768fs (~ 48kHz)	64fs

Table 2：Mode Select

Note： SDTO outputs 16bit data at SCLK=32fs.

8.2. Audio Interface Format

Two kinds of data formats can be chosen with the DIF pin(Table 3)。In both mode of CKS2-0，the serial data can be set to MSB or I2S format。The SDTO is clocked out on the falling edge of SCLK.the audio interface supports both master and slave modes.In master mode, SCLK and LRCK are output with the SCLK frequency fixed to 64fs and the LRCK frequency fixed to 1fs.

Mode	DIF pin	SDTO	LRCK	SCLK	Example
0	L	24bit,MSB justified	H/L	≥48fs or 32fs	Figure 7
1	H	24bit,I2S compatibel	L/H	≥48fs or 32fs	Figure 8

Table 3：Audio Interface Format

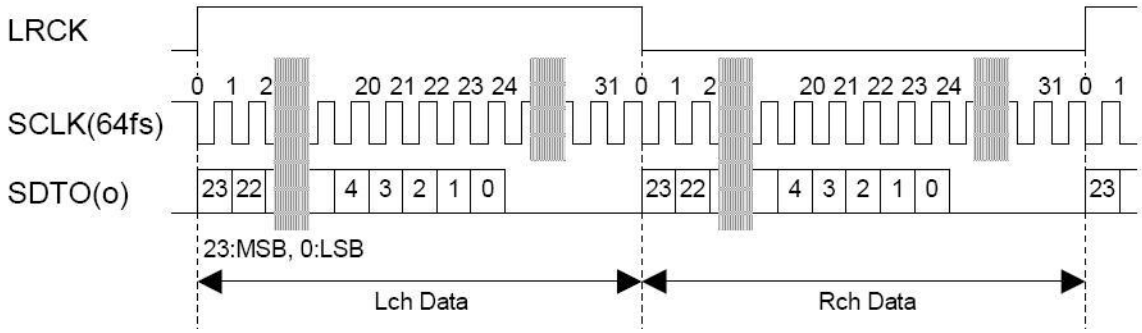

Figure 7 . Mode 0 Timing

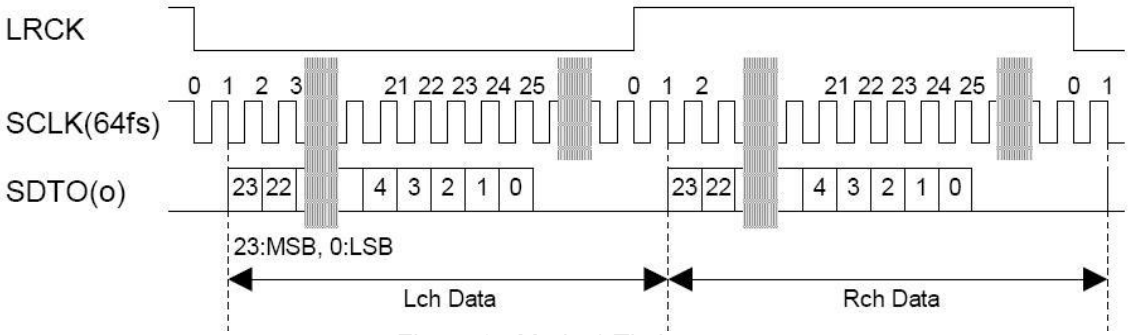

Figure 8 . Mode 1 Timing

8.3. Digital High Pass Filter

The ADC has a digital high pass filter to to remove DC offset .The cut-off frequency of the HPF is 1.0Hz (@fs=48kHz) ,cut-off frequency is proportional to sampling rate (fs).

HPF is controlled by CKS2-0 pin （Table 2）. If HPF setting(ON/OFF) is changed when the CJC5357B is in operation,click noise occurs by changing DC offset .It is recommended that HPF setting is changed when the PDN=”L”.

8.4. Power Down

The CJC5357B is placed in the power-down mode by bringing the PDN pin “L”and the digital filter is also reset at the same time .This reset should always be executed after power-up .In the power-down mode, the VCOM is the same voltage as AGND.An analog initialization cycle starts after exiting the power-down mode. Therfore, the output data SDTO becomes available after

4051 cycles of LRCK clock in master mode or 4233 cycles of LRCK clock in slave mode .During initialization, the ADC digital output data of both channels are forced to a 2’S complement“0”。
The ADC output setting in the value corresponding to the input signals after the initialization was completed.

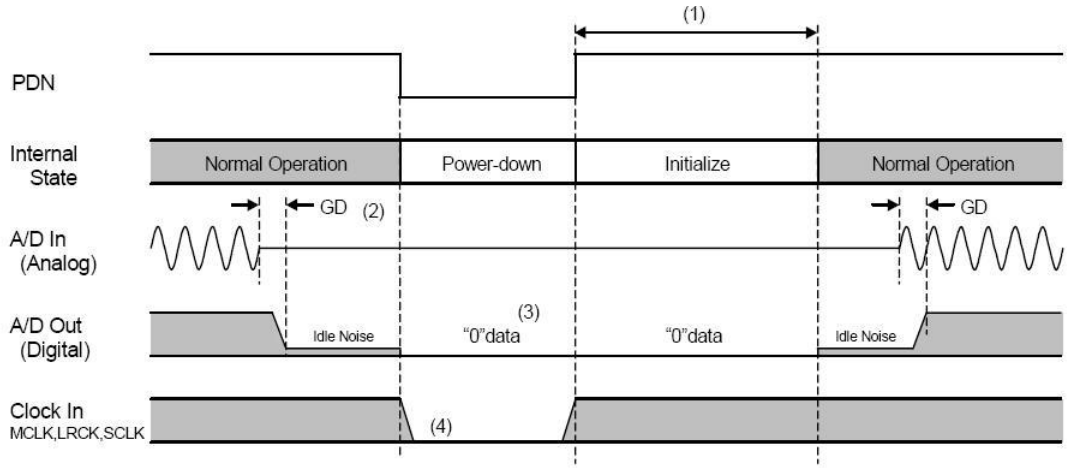

Figure 9 CJC5357B Power-up/Power –down Timing

Note ：

(1) 4233/fs in slave mode and 4051/fs in master mode .

(2) Digital output corre sponding to analog input has the group delay .

(3) A/D output is “ 0”data at the power-down state.

(4)When the external clocks （MCLK,SCLK,LRCK）are stopped，CJC5357B should be in the power-down state.

8.5. System Reset

The CJC5357B should be reset once by bringing the PDN pin“L” after power-up. In slave mode ,the internal timing starts clocking by the rising edge (falling edge at mode 1) of LRCK after exiting from reset and power down state by MCLK .The CJC5357B is power down state until LRCK is input .In master mode,the internal timing starts when MCLK is input.

9. System design

Figure 10 show the system application diagram.

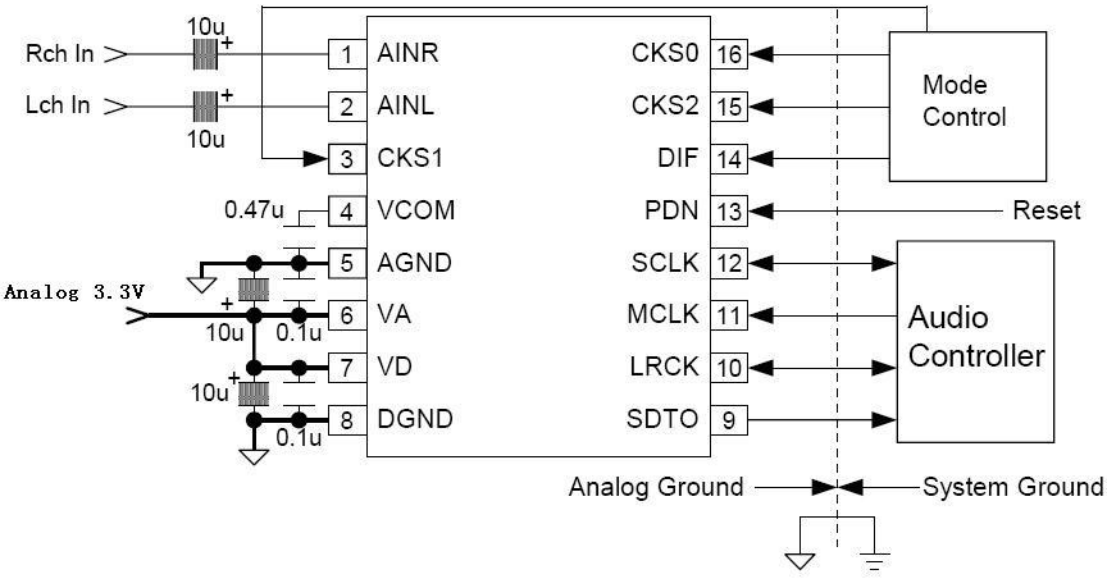

Figure 10 CJC5357B System Application Diagram

Note ：

(1) AGND and DGND of the CJC5357B should be distributed separately from the ground of external digital devices(MPU,DSP).

(2) All digital input pins should not be left floating.

(3) The CSK1 pin should be connected to VA or AGND.

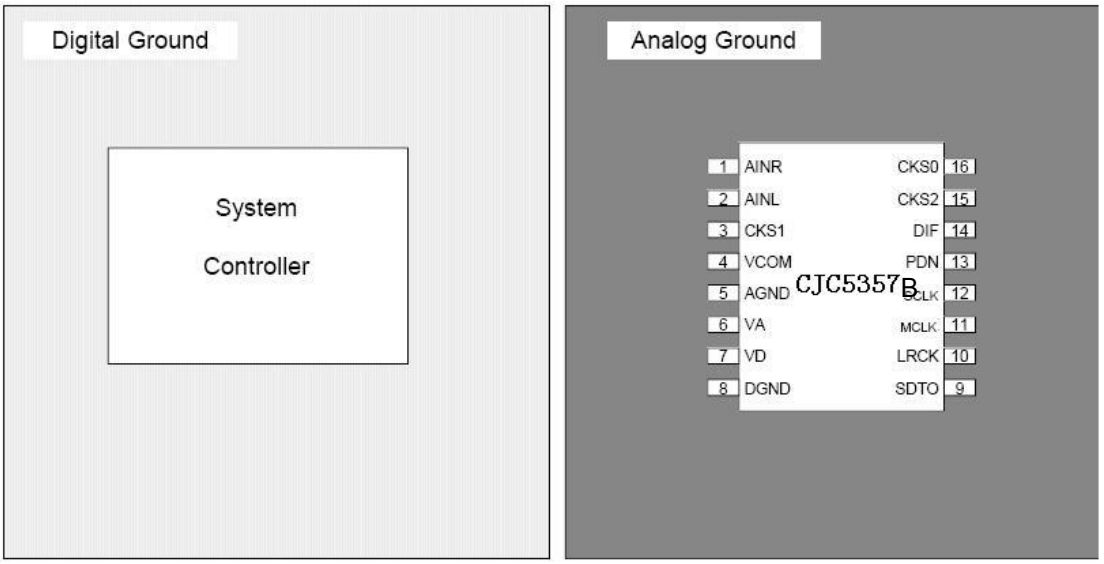

Figure 11 Ground Layout

Note ： AGND and DGND must be connected to the same analog ground plane.

9.1. Grounding and Power Supply Decoupling

The CJC5357B requires careful attention to power supply and grounding arrangements.If VA and VD are supplied separately,the power-up sequence is not critical. AGND and DGND of the CJC5357B must be connected to analog ground plane. Systerm analog ground and digital ground should be connected togerther near to where the supplies are brought onto the printed circuit board. Decoupling capacitors should be as near to the CJC5357 as possible, with the small value ceramic capacitor being the nearest.

9.2. Voltage Reference

The voltage input to VA sets the analog input range.VCOM are 50% VA and normally connected to AGND with a 0.1μF ceramic capacitor.A ceramic capacitor 0.47μF attached to VCOM pin eliminates the effects of high frequency noise .NO load current may be drawn from these pins. All signals, especially clocks,should be kept away from the VCOM pin in order to avoid unwanted coupling into the CJC5357B.

9.3. Analog Inputs

The ADC inputs are single-end and internally biased to the common voltage with 20Kohm resistance. The input signal range scales with the supply voltage and nominally 0.85*VA Vpp(typ). The ADC output data format is 2's complement. The DC offset is removed by the internal HPF.

The CJC5357B samples the analog inputs at 64fs.The digital filter rejects noise above the stop band except for multiples of 64fs.The CJC5357B includes an anti-aliasing filter（RCfilter） to

attenuate a noise around 64fs.

10.Package

16pin TSSOP(Unit:mm)

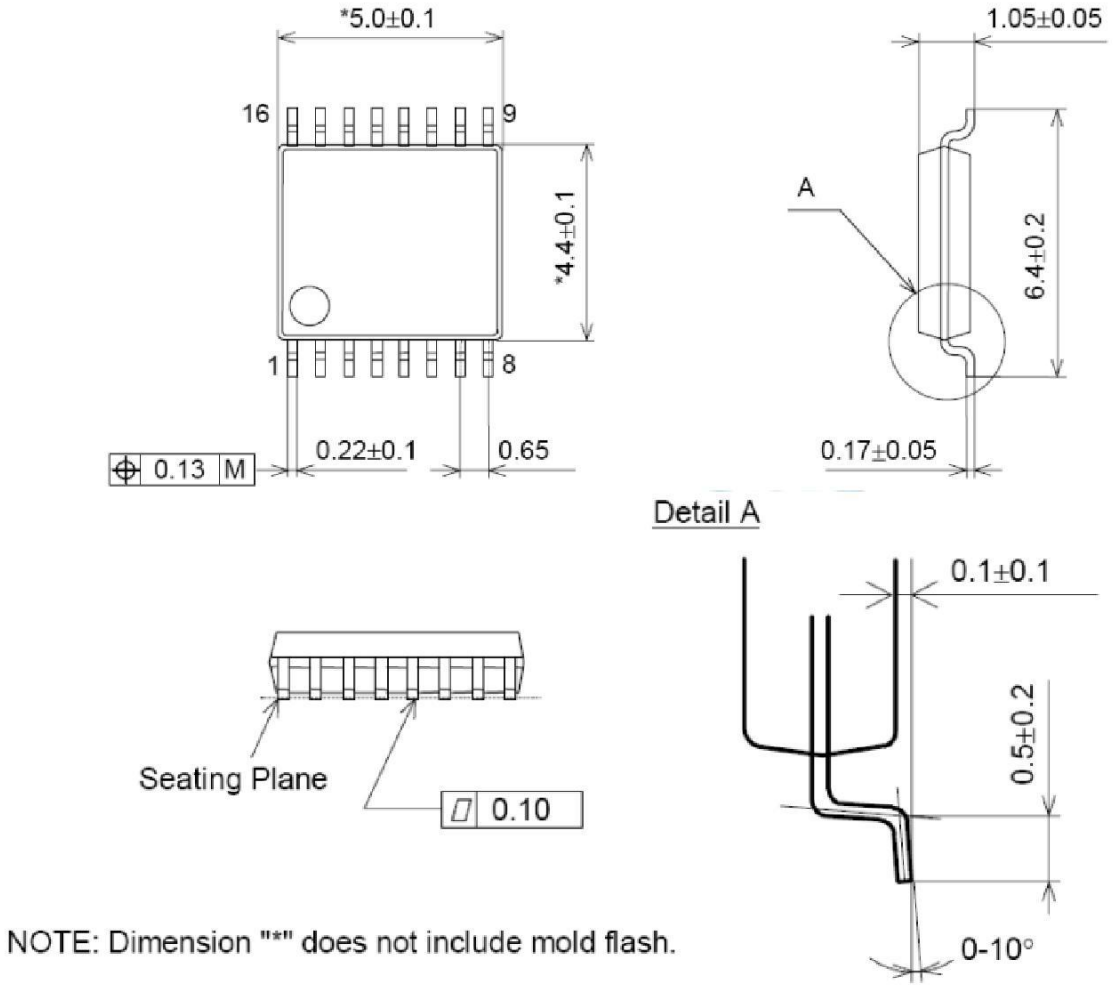

Figure13. CJC5357B Package Size